Abstract: Gallium arsenide junction field-effect transistors (GaAs JFETs) can be made immune to carrier freeze-out, making such transistors useful for the readout of detectors arrays that operate at 4 K. Typical applications require transistors with very low noise and extremely low leakage currents. By using a recently developed etchant for GaAs that is highly isotropic, etched GaAs JFETs have fabricated that have a gently tapered edge. This reduces edge fields and consequently reduces the edge tunneling current, which is responsible for virtually all of the gate leakage current at 4 K. JFETs with gate leakage currents below 10^{-15} amps have been fabricated. The fabrication technique, including the isotropic etchant are discussed. The leakage current and noise of these JFETs is presented and compared with previous devices using a conventional etch.

1. INTRODUCTION

Future American and European space missions will employ detectors cooled to below 4 K. This includes detectors for the very long wavelength infrared (VLWIR, approximately 50 μm to 200 μm wavelength). It also includes normal and low temperature superconducting bolometers for submillimeter wave, infrared, and X-rays. For small arrays consisting of less than ten pixels, it had been adequate to cool only the detector array to 4 K, and to run a wire from each pixel to a warmer compartment containing the readout electronics. These wires carry heat to the cold head, however, and they are susceptible to noise pickup, which makes this approach impractical for larger arrays or for ultra-low noise levels.

Therefor, several different groups have been exploring readout electronics that can operate at 4 K and below, and that can be placed on the cold head immediately adjacent to the detector array[1-5]. Clearly such electronics must circumvent carrier freeze-out and be functional at 4 K. In addition, the electronics must be low power, so as not to dissipate excessive heat onto the cold head. Finally, since space-based IR detectors are typically high impedance and produce small signals, the readout electronics must have low input bias currents and low noise. For the Space Infrared Telescope Facility (SIRTF), for example, the readout electronics is required to dissipate less than 10 μW per channel, have less than 00 electrons per second input currents, and have an input-referred voltage noise of less than 1 $\mu V/Hz^{1/2}$ at Iz.

We have been exploring GaAs JFET-based electronics for such applications for the past several years[6]. Because of the very small electron effective mass in GaAs, n-type GaAs can be made immune to carrier

freeze-out at moderate doping levels that still allow depletion. A p^+ on n GaAs JFET is immune to freeze-out, and functions normally at 4 K. In addition, the large barrier provided by the p-n junction in the JFET reduces the gate leakage current relative to metal Schottky gate FETs (MESFETs).

The principal challenge has been to reduce the noise and gate leakage current to acceptable levels

2. THE DEVICE STRUCTURE.

The device structure is shown in Fig. 1. The device consists of an n-type layer on top of an undoped layer on a semi-insulating substrate. There is a p-type layer on the n-layer to form the gate. The layer structure is grown by MBE. Then wet chemical etching is used to etch back the layers. One etch is used to etch away the p-gate and expose the n-layer. Another etch is used to etch through the n-layer to isolated devices. Nickel-germanium-gold (Ni-Ge-Au) metalization is deposited on the n-layer and alloyed at 400°C to form the ohmic contacts, and titanium-platinum-gold (Ti-Pt-Au) non-alloyed metal is used to contact the gate. A Polyamide dielectric is deposited over the entire structure, with contact holes opened in it by plasma etching. A chromium-gold metal is used to bring the source, gate, and drain contacts out to pads for wire bonding.

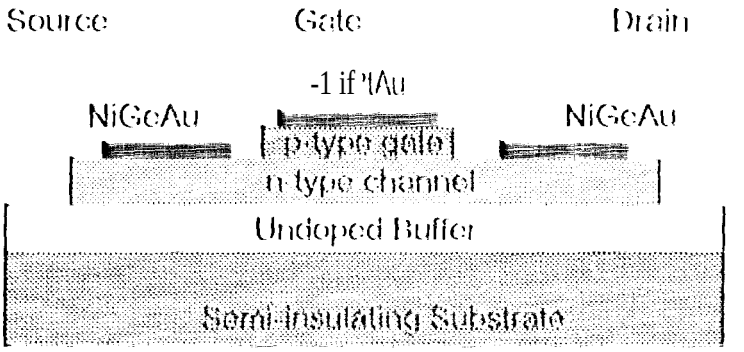

Fig. 1: The structure of the GaAs JFET produced by MBE growth and etch-back. The undoped buffer is approximately 1 μm thick. The n-type channel is several thousand angstroms thick and doped with silicon to between 1×10^{16} to 1×10^{17} cm^{-3}. The p-type gate is 500 Å thick and is doped to greater than 5×10^{18} cm^{-3}. Alloyed Ni-Ge-Au is used to make contact to the n-type regions for the source and drain. Non-alloyed Ti-Pt-Au is used to contact the p^+ gate.

3. OLD AND NEW GATE ETCH PROCEDURES.

Previously devices were made using a self-aligned gate etch and an ammonium hydroxide based etch. That is, the Ti-Pt-Au was patterned by lift-off, during which the photoresist was removed. The Ti-Pt-Au metal contact was then used as the mask to pattern the etch that defined the gate. The etchant was a mixture of ammonium hydroxide, hydrogen peroxide and water (1:1:4:550 by volume). The same etchant was used to make the isolation etch, using a photoresist mask.

This procedure requires only one mask level to create the gate, and it resulted in functional devices. However, there were several problems with it. First, there is some edge roughness in the gate metalization due to the nature of the lift-off process. This edge roughness is duplicated by the etch in the self-aligned process. There is also some undercut, and metal filaments can fall over the edge of the gate, forming a Schottky barrier between the gate metalization and the n-type channel. The surface roughness tends to enhance the field in localized spots. Both the field enhancement and the parasitic Schottky contacts tend to increase the leakage current.

For this reason, we began fabricating devices using a second procedure. In this procedure, a photoresist mask is used to mask the gate etch. The gate metalization is still done using lift-off, but in a separate step

rather than self-aligned as in the previous procedure. The mask set is designed so that the gate metal edge falls by several microns inside the edge of the p-type GaAs formed by the gate etch.

Additionally, the chemistry of the wet chemical etchant was changed. Mixtures of hydrogen peroxide and an acid or base all work by using the hydrogen peroxide to oxide the GaAs to form gallium oxide and arsenic oxide. These oxides are then dissolved by the acid or base. Even in dilute mixtures, however, these etches are not perfectly isotropic, and can result in a retrograde etch wall profile on the 110 faces.

It is believed that the anisotropy results because the arsenic oxides tend to dissolve more readily than the gallium oxide. In fact, arsenic oxide has some solubility even in pure water. Because the arsenic oxide is removed preferentially, the gallium oxide accumulates until its dissolution becomes a rate limiting step. The etch becomes rate limited rather than diffusion limited, and consequently the etch becomes orientation dependent.

A new, more isotropic etchant has recently been developed based on an hydrofluoric acid/ hydrogen peroxide/ water system[7]. The peroxide oxidizes the GaAs as before. It is believed, however, that HF naturally has more of an affinity for gallium oxide. In a dilute solution, this counters the natural tendency for the arsenic oxide to dissolve faster, making the dissolution rates roughly equal. This keeps the etch diffusion limited and consequently isotropic.

The concentration of 2:10:1000 $HF:H_2O_2:H_2O$ was used for the gate etch. The etch rate is approximately 200" Å/min. A slightly less dilute concentration of 2:10:200 was used for the mesa etch. The etch rate of this solution is approximately 2000 Å/min.

4. A COMPARISON OF JFETS FABRICATED BY THE OLD AND NEW PROCEDURES.

The gate leakage current vs. gate voltage of JFETs fabricated using the self-aligned procedure and NH_4OH-based etchant was measured using the circuit shown in Fig. 2a. The results for a ring geometry JFET 20 μm wide and 1250 μm in circumference is shown in Fig. 3. The current rises above 1 pA at a gate voltage of approximately -6.5 V, and increases to almost 1 nA at a gate voltage of -10 V. The current noise floor of the system is approximately 1 pA.

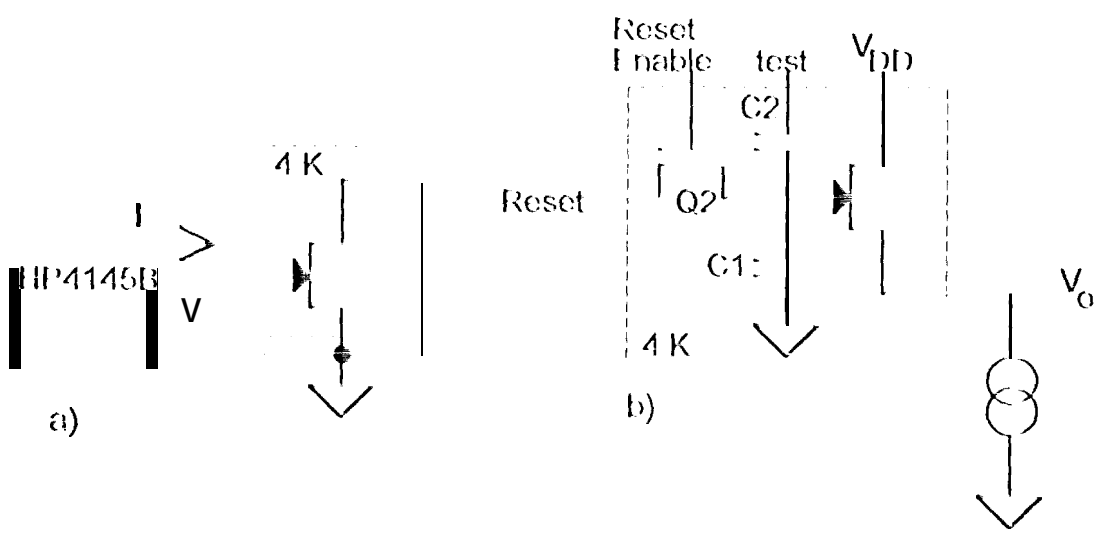

Fig. 2: The circuits used to measure leakage current. Circuit 2a uses a HP4145B semiconductor parameter analyzer as an ammeter to measure gate leakage vs. voltage down to 1 pA. Circuit 2b uses the JFET as a source-follower, and integrates the leakage current onto the capacitor C. The time rate of change of V_o is proportional to the leakage current. The sensitivity is limited by the drift noise to about 10^{-16} amps.

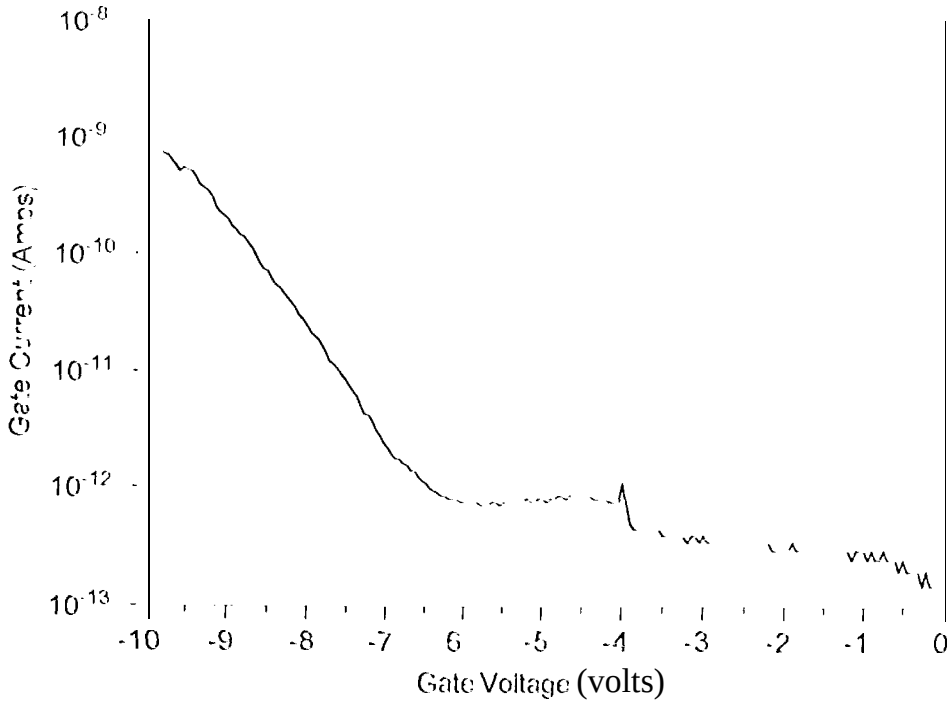

Fig. 3: The gate leakage current as a funtion of voltage for a ring JFET 1250 μm in circumference and 20 μm long that was made using the old process using the gate metalization as an etch mask, and using an ammonium hydroxide-based etchant. The source and drain are grounded for this measurement.

The current of a rectangular JFET fabricated using the separate gate etch and metalization and using the HF-based etchant was also measured using the circuit of Fig. 2a, but the resulting current was less than 1 pA out to a gate voltage of -15 V. To measure the gate current of this device, it was necessary to use the circuit shown in Fig. 2b. In this circuit, the JFET under test is connected as a source follower. A reset voltage is applied onto the gate of the JFET by turning on Q2, and this voltage is stored on capacitors C1 and C2. At the start of the integration period, Q2 is turned off, and the gate leakage current of the JFET is integrated on the capacitor set. The change in the gate voltage is reflected in the change of the source follower voltage. The gate leakage current can then be calculated from the rate of change of the source follower voltage using Eq. 1.

$$I_{leakage} = \frac{C_T}{A_v} \frac{d}{dt} V_o \qquad \text{Eq. 1}$$

where A_v is the gain of the source-follower, and C_T is the total capacitance of $C1$ and $C2$, together with the capacitance of the gate of the JFET and including any parasitic capacitance.

For this measurement, C1 and C2 were both 1 pF. The reset voltage was 1 V, and V_{DD} was set to 3 V. The load bias current on the source of the JFET was 10 μA.

For an accurate calculation of the leakage current, both C_T and A_V must be measured. The gain A_V was measured by turning on Q2 and sweeping the Reset voltage from 0 to ? V and recording the output voltage V_o. With a 10 μA load current, the output voltage varied from 1.213 to 3.1oO V as the input was swept from 0 to 2 V. This implies that the gain of the source follower circuit is A_v = 0.9435.

The capacitance was measured by injecting a 1 kHz AC signal only the test point connected to C2. The circuit then forms a capacitive divider between C2, and the remaining capacitance C_X, as shown in Fig. 4. C_X is the sum of C1, the capacitance of the JFET, and any parasitic capacitance.

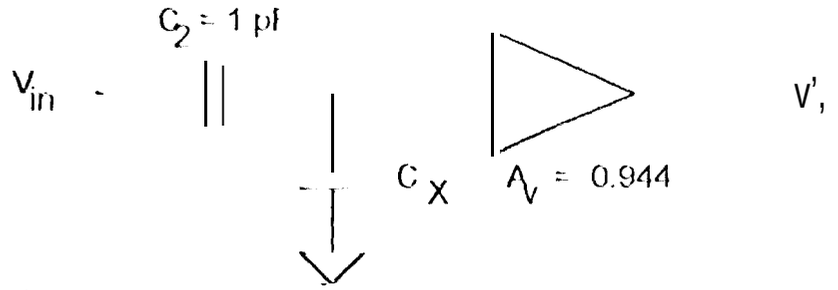

Fig. 4: The equivalent capacitive divider circuit that results from injecting an AC signal on to the test node of the circuit of Fig. 2b.

$$o = A_v \frac{C2}{C_X + C2} V_{in} \quad \text{Eq. 2}$$

$$C_X = \frac{A_v V_{in} - V_o}{V_o} C2 \quad \text{Eq. 3}$$

When a 1 V amplitude, 1 kHz sine wave was injected at the test point, the corresponding amplitude of the output voltage was 0.040 V. Using the gain of 0.944 and the value of C2 = 1 pF, C_X can be calculated to be 22.6 pF. This indicates that there the parasitic capacitance is actually dominant, since the capacitance of C1 is only 1 pF, and the capacitance of the JFET is calculated to be 0.35 pF.

For the leakage test, the injection test point connected to C2 is grounded, so the total capacitance C_T is the sum of C2 and C_X, or C_T = 23.6 pF.

The output voltage vs. time for the JFET is shown in Fig. 5, The output voltage varies by approximately 41 mV over the 29 minute integration time. Using the calculated gain and capacitance with Eq. 1, the calculated leakage current is:

$$I_{leakage} = 0.59 \text{ fA} \quad \text{Eq.4}$$

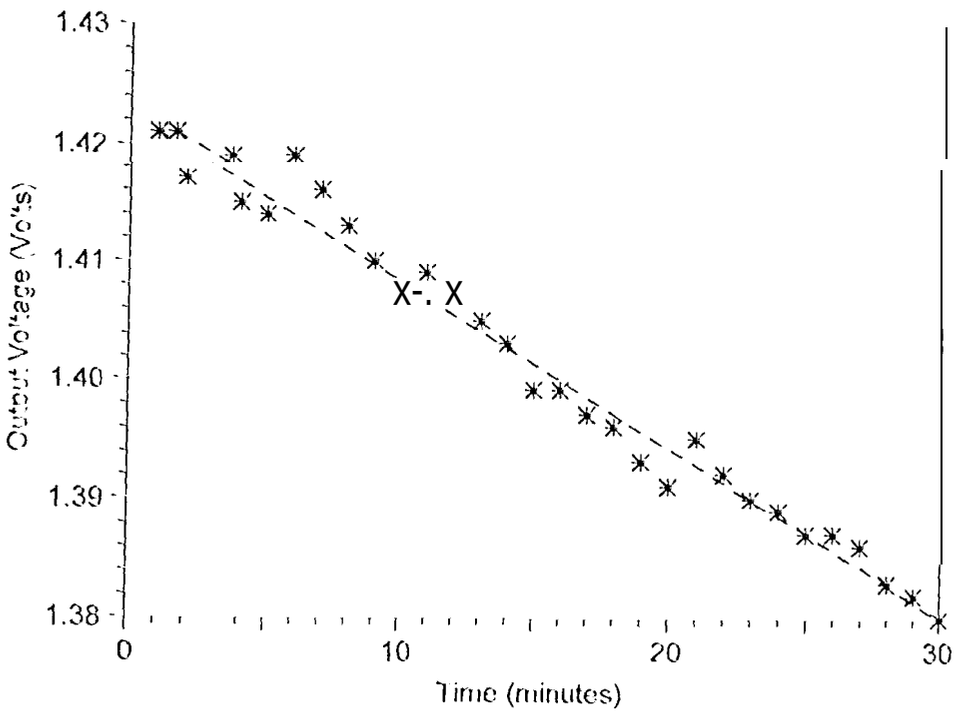

Fig. 5: The source-follower output voltage V_o from the circuit shown in Fig. 2b, as a function of time for a rectangular JFET fabricated using the new process using a separate gate metalization and etch and using an HF-based etchant. The total capacitance was measured as 23.6 pF.

5. THE TRANSISTOR NOISE FOR THE OLD AND NEW PROCEDURES

The input-referred voltage. noise for a JFETs fabricated using the old process and two JFETs fabricated using the new process are compared in Fig. 6. The old JFET was a ring structure 1250 μm in diameter and 20 μm long. The new JFETs are rectangular structures, one king 300 μm wide and 100 μm long with a capacitance of 21 pF, and the other being 20 μm wide and 25 μm long with a capacitance of 0.35 pF. All of the devices were biased at 1 μA drain current. The drain voltage was 1.0 V for the old JFET and **0.6** V for the new JFETs.

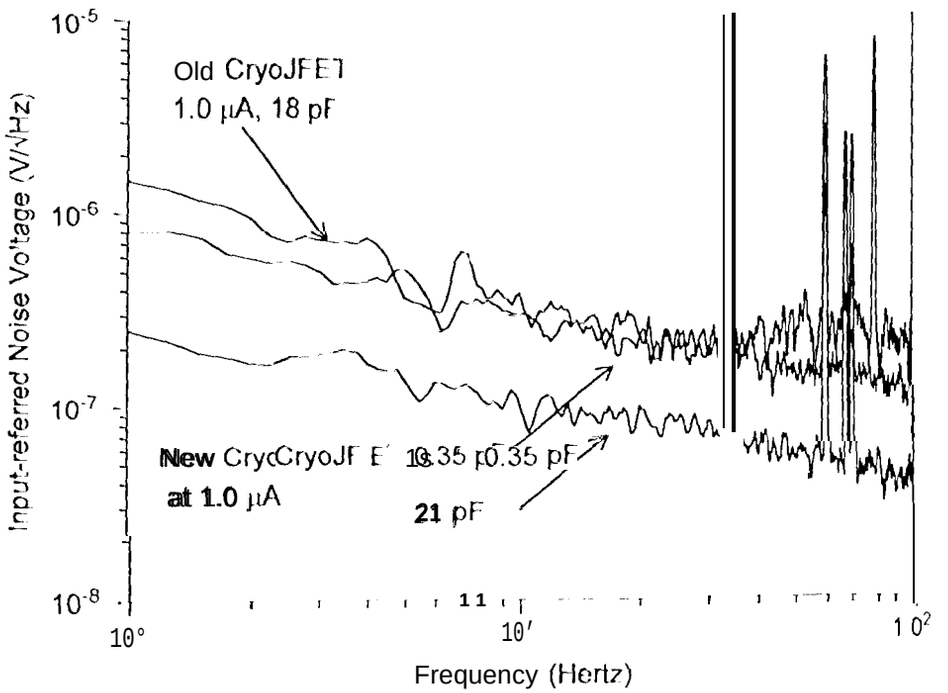

Fig. 6: The input-referred voltage. noise for a ring JFET (1 250 μm circumference by 20 μm long) fabricated with the old process using the gate metalization as a mask and an ammonim bydroxidc-based etch, and the comparable noise for rectangular JFETs (300 pm wide by 100 μm long and 20 μm wide by 25 μm long) fabricated with the new' process using a separate gate etch and metalization and using an IJF-based etch. The noise spikes are 60-Hz pickup and signals injected to calibrate the gain.

6. SUMMARY

A new gate etch process has been developed that substantially improves the performance of JJF11'1's intended for deep cryogenic operation. Where before the etch was done using an ammonium hydroxide-based etchant and using the gate metalization as a mask, the new procedure separates the photolithography for the gate etch and the gate metalization into two steps. In addition, a more isotropic 1 IF-based etch is used. The new procedure reduced the gate leakage by many orders of magnitude, from leakage on the order of pA to less than a fA. The noise is also reduced significantly.

The noise and leakage performance are closing in on those required for deep cryogenic space astronomy missions such as SIRTF. The fabrication of more JFETs using the new procedure, and further characterization of their gate leakage current and noise are under way,

7. ACKNOWLEDGMENTS

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8. REFERENCES

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